

2 / 8

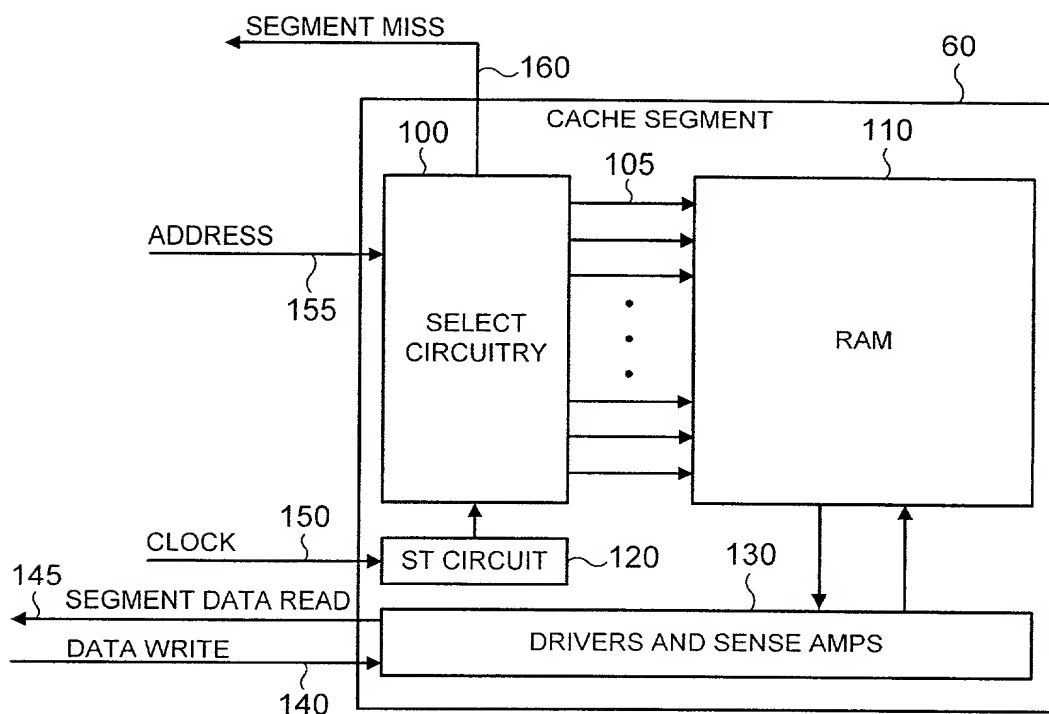


FIG. 2

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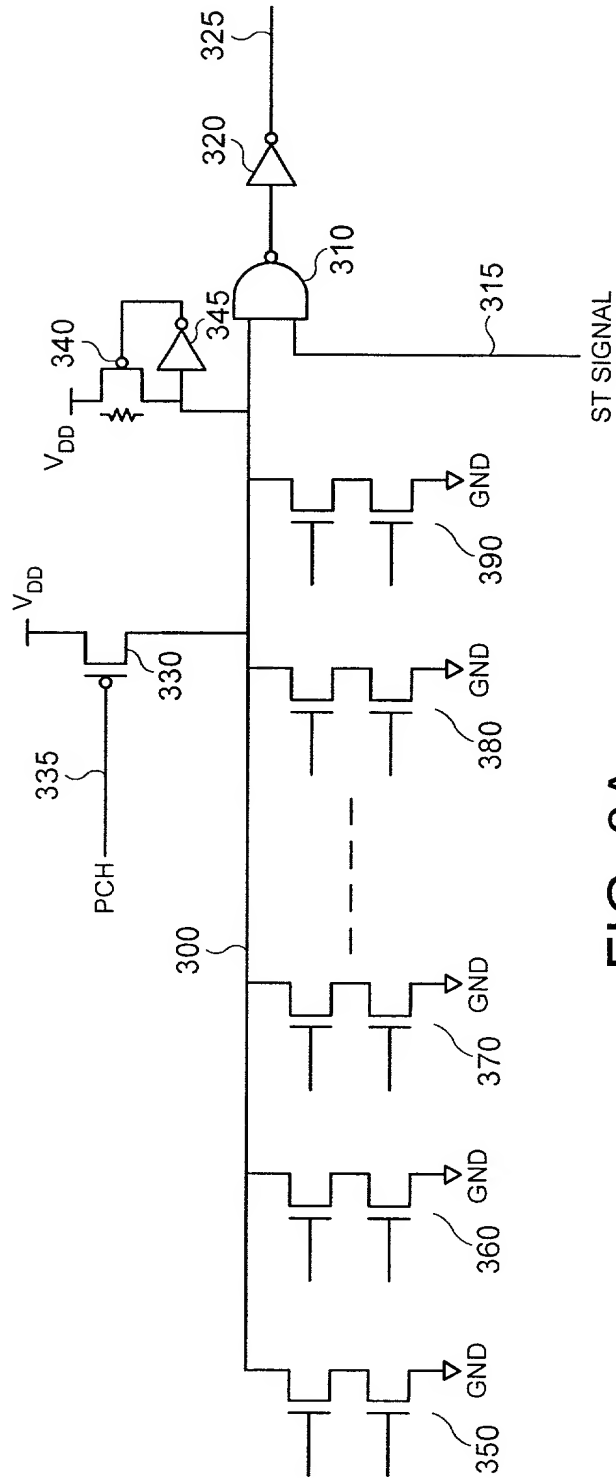


FIG. 3A

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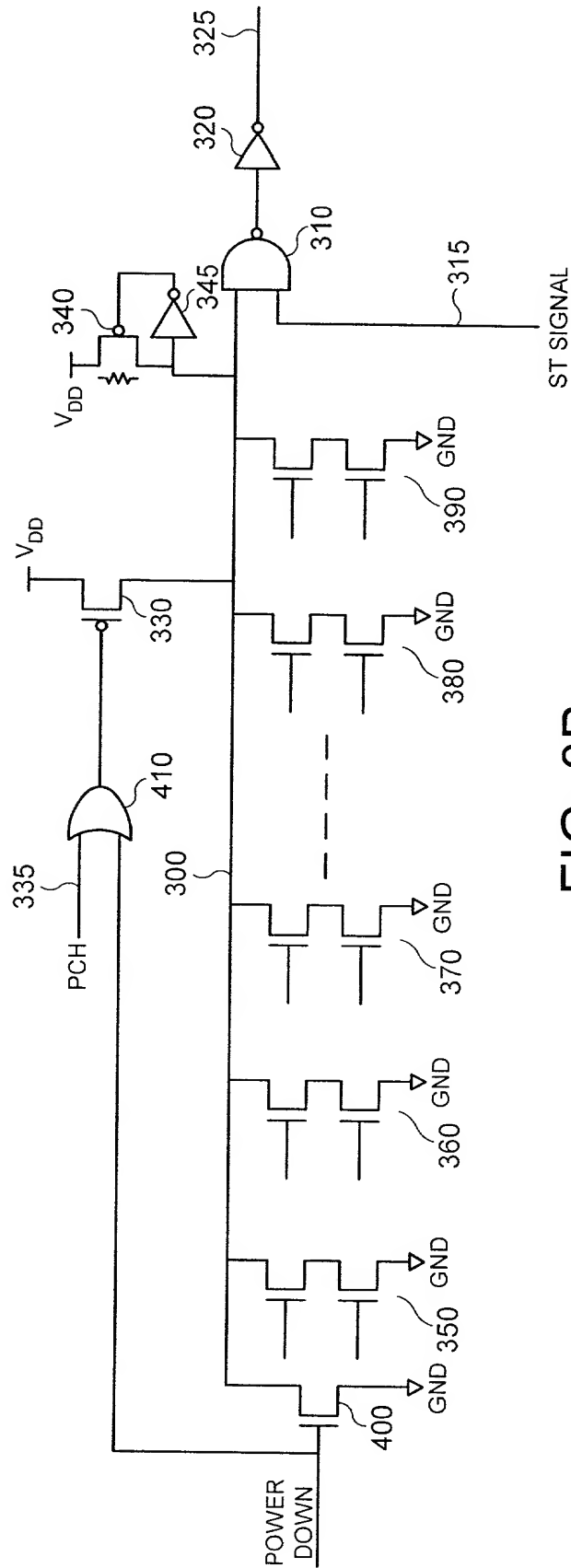


FIG. 3B

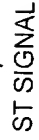


FIG. 3C

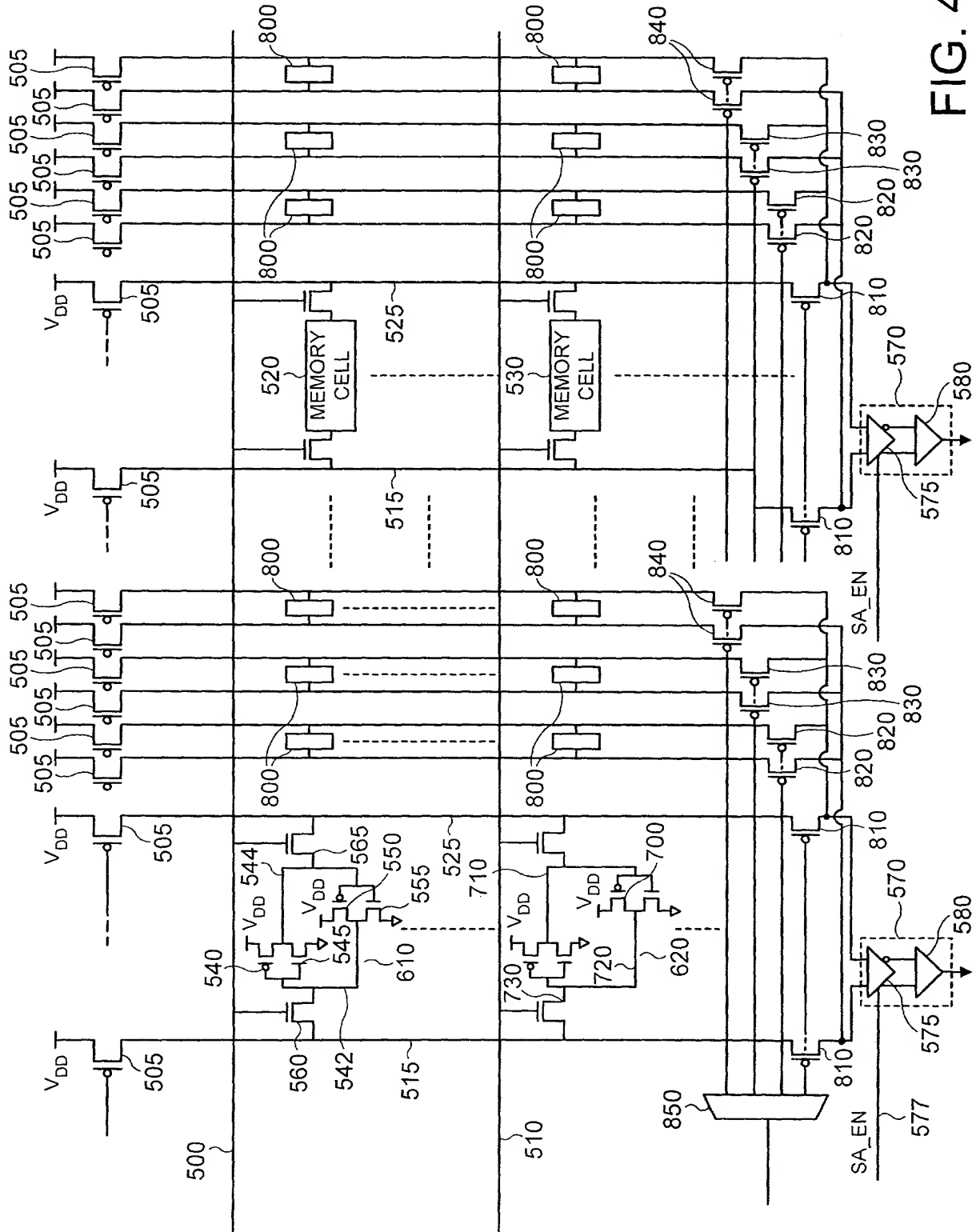


FIG. 4A

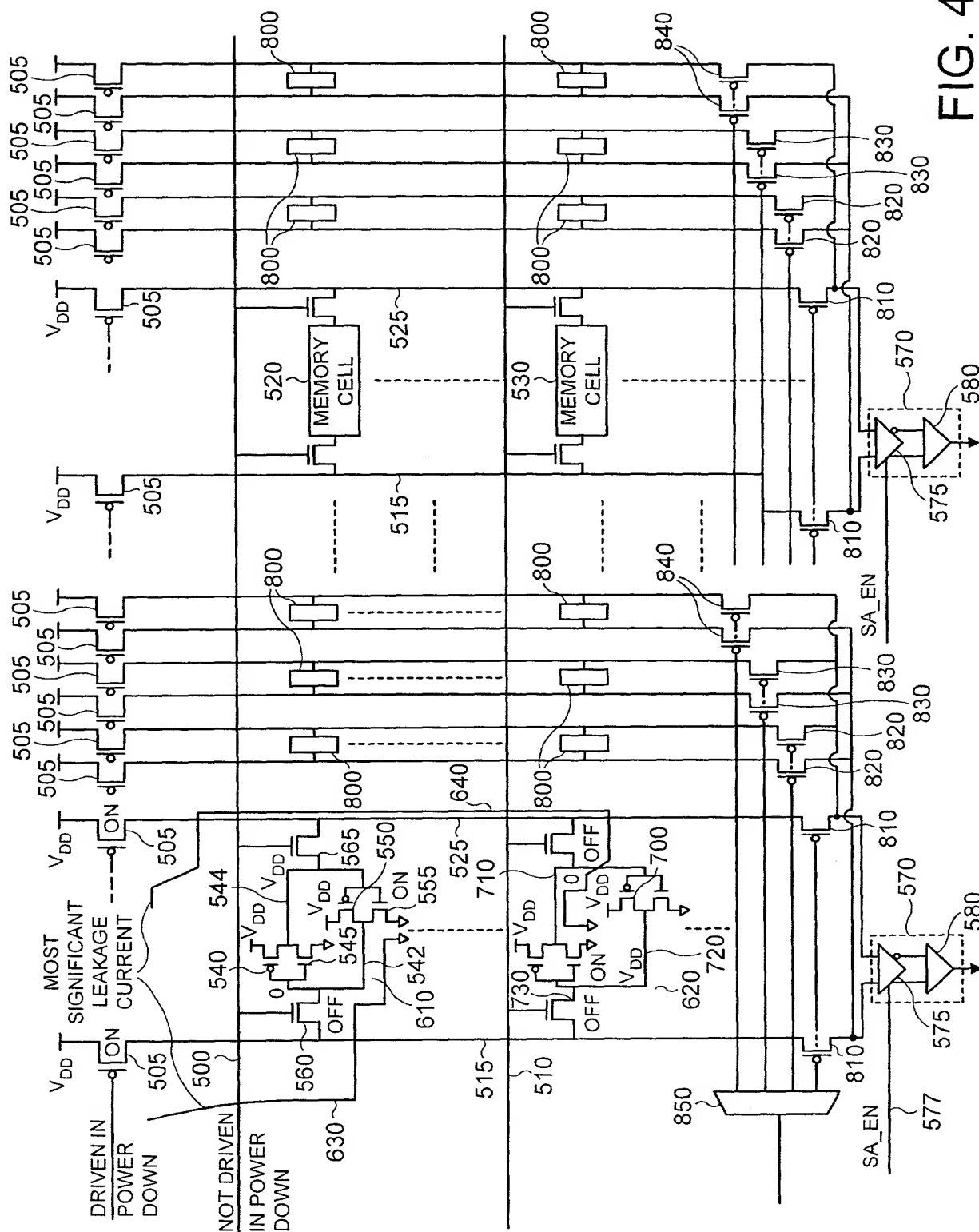


FIG. 4B

FIG. 4C is a schematic diagram of a memory array in a power-down state. The array includes a word line driver 600, a word line 505, a bit line 800, and a memory cell 520. The word line driver 600 is controlled by a power-down signal PCH. The word line 505 is connected to the memory cell 520. The bit line 800 is connected to the memory cell 520. The memory cell 520 is connected to the bit line 800. The array is shown in a power-down state, where the word line driver 600 is turned off and the memory cell 520 is in a high-impedance state.

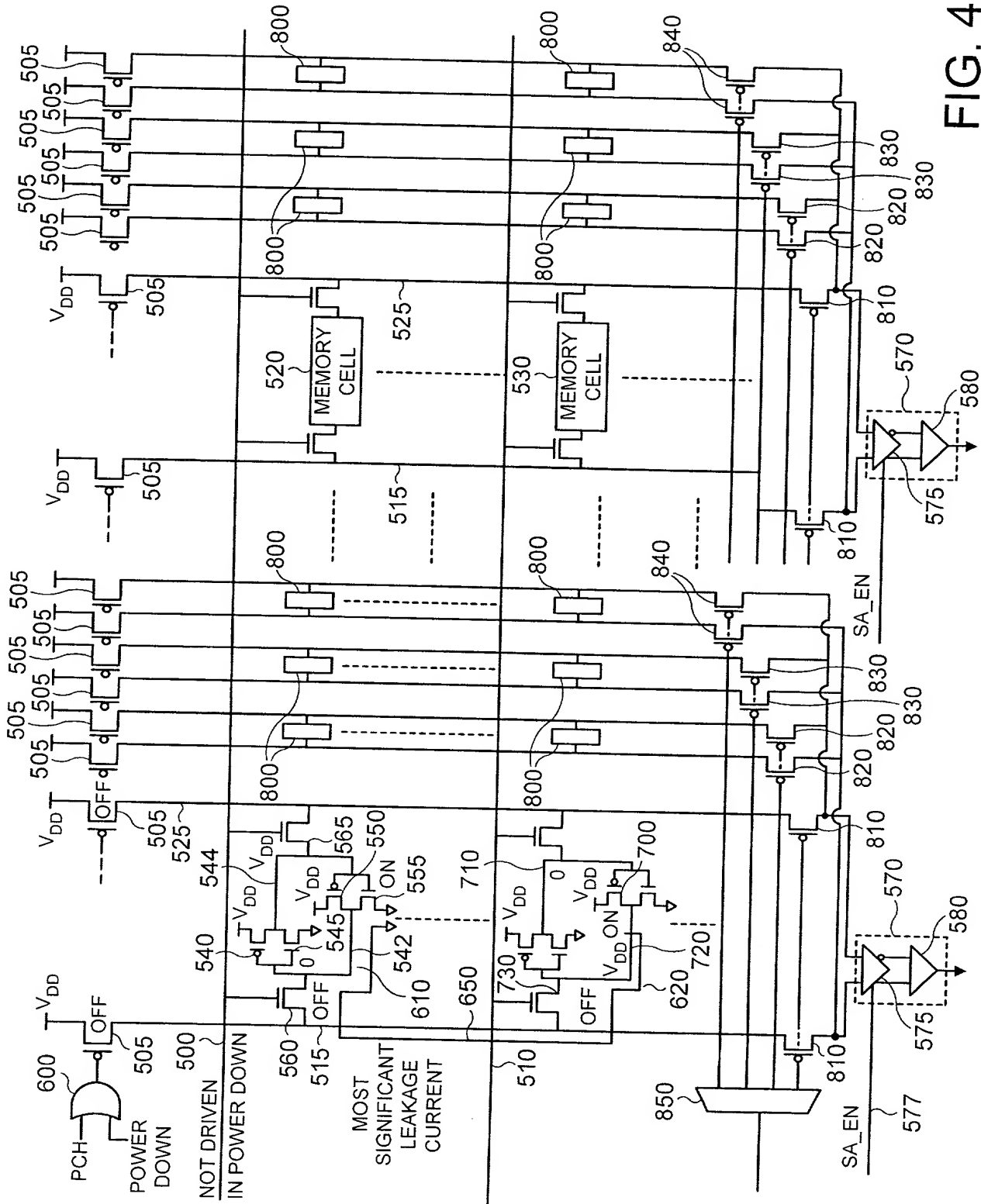


FIG. 4C